

REMARKS

Claims 1-4, 11, 18 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. (U.S. Patent 6,541,382) in view of Ballantine et al. (U.S. Patent 6,417,070), and further in view of either Hanratty et al. (U.S. Patent 6,930,028) or Tobben et al. (U.S. Patent 6,103,456). This rejection is respectfully traversed for the following reasons.

Claim 1 recites, "patterning a silicon oxynitride layer having a composition $\text{Si}_x\text{O}_y\text{N}_z\text{H}_A$ " and "conditioning the patterned silicon oxynitride layer such that the silicon oxynitride layer has a composition $\text{Si}_x\text{O}_y\text{N}_z\text{H}_A$ ". (Emphasis added.)

Hanratty et al. and Tobben et al. are cited to support the argument that the silicon oxynitride layer of Cheng et al. could include hydrogen as recited by Claim 1. However, the primary argument still seems to be related to Cheng et al. and Ballantine et al.

The Examiner indicates that one of ordinary skill would "combine the teachings of Ballantine et al. with Cheng et al. because it would enable formation of thermal oxide layer 70a of Cheng et al."

The rapid thermal anneal (RTA) parameters of Ballantine et al. are selected to provide a particular radius of curvature at the corners of the liner 8. (Ballantine et al., Col. 2, lines 53-56, Fig. 9.) Ballantine et al. teach that the radius of curvature of the top isolation trench corner is critical to the threshold voltage of the resulting CMOS FET device. (Ballantine et al., Col. 2, lines 25-29.) Ballantine et al. requires lateral erosion (PB) of the overlying insulating layer 3 in order to achieve the desired

rounding of the top isolation trench corner. (Ballantine et al., Col. 2, lines 21-25; Figs. 7-9.)

The first and second embodiments of Cheng et al. require a recessed hardmask (See, Figs. 1D and 2A), which is similar to the laterally eroded insulating layer 3 required by Ballantine et al. However, the first and second embodiments of Cheng et al. cannot be relied upon by the Examiner (as these embodiments teach away from Applicant's claimed invention). Thus, the Examiner's rejection must rely on the third embodiment of Cheng et al. However, Cheng et al. explicitly states that the third embodiment "omits the recession of the silicon nitride" hardmask. (Cheng et al., Col. 7, lines 60-62.) Because the third embodiment of Cheng et al. explicitly omits the recessed hardmask, it is not obvious to use the RTA parameters of Ballantine et al. (which are used to provide a specified corner rounding with a recessed hardmask), in the third embodiment of Cheng et al. For this reason, it is not obvious to combine Cheng et al. and Ballantine et al.

In addition, the RTA parameters of Ballantine et al. are used to form a silicon oxide liner 8. (Ballantine et al., Col. 2, lines 30-56.) However, the Examiner requires that the RTA parameters of Ballantine et al. be used to form the sacrificial oxide layer 70a of Cheng et al., which is a different element than the silicon oxide trench liner 72a of Cheng et al. Thus, the Examiner is using the RTA parameters of Ballantine et al. for a different purpose (and to form a different element) than that described by Ballantine et al. For this reason, it is not obvious to use the RTA parameters of Ballantine et al. to form the sacrificial oxide layer 70a of Cheng et al.

In addition, the Examiner indicates that Cheng et al. does not disclose that a rapid thermal anneal is performed for about 20 seconds at a temperature of about 900°C (as recited by Applicant's Claim 4). The Examiner looks to Ballantine et al. to provide these rapid thermal anneal parameters. However, in discussing the rapid thermal anneal parameters, Ballantine et al. explicitly state that it is "understood that the time is inversely related to the temperature". (Ballantine et al., Col. 2, lines 40-41.) Thus, Ballantine et al. explicitly teach that the lower temperatures of the range (i.e., 900°C) should be associated with the longer times in the range (i.e., three minutes). Ballantine et al. also specify a smaller preferred range of temperatures (1050°C to 1200°C) and a smaller preferred range of times (20 seconds to 1 minute). (Ballantine et al., Col. 2, lines 33-40.) Using the stated inverse relationship of Ballantine et al., a rapid thermal anneal at a temperature of 1050°C (lowest temperature in the cited range) should be performed for about 1 minute (longest time in the cited range); and a rapid thermal anneal at a temperature of 1200°C (highest temperature in the cited range) should be performed for about 20 seconds (shortest time in the cited range). By specifying the inverse relationship of time and temperature, Ballantine et al. teach away from a rapid thermal anneal at temperature of 900°C for about 20 seconds.

Moreover, Cheng et al. specifically requires that the silicon oxynitride layer be converted to silicon oxide. (Cheng et al., Col. 8, lines 20-27.) Thus, even if the RTA parameters Ballantine et al. resulted in the formation of conditioned silicon oxynitride as suggested by the Examiner, Cheng et al. explicitly teach away from using such RTA parameters. Stated another way, even if it were proper to

combine Cheng et al. and Ballantine et al., and such combination resulted in the formation of a conditioned silicon oxynitride layer, the resulting method would fail to meet the specifications of Cheng et al., which include converting the silicon oxynitride layer 16 into silicon oxide. The Examiner is effectively arguing that one must use a method of growing a silicon oxide liner disclosed by Ballantine et al. to grow the sacrificial silicon oxide layer 70a in Cheng et al., but then fail to convert the corresponding silicon oxynitride layer 16 into silicon oxide as specified by Cheng et al., and rather, produce the conditioned silicon oxynitride layer as recited by Applicant's Claim 1. The Examiner's argument therefore requires the combination of Cheng et al. and Ballantine et al. to fail to operate as specified by Cheng et al. This failure also teaches away from combining Cheng et al. and Ballantine et al.

For the above-cited reasons, Claim 1 is allowable over Cheng et al. in view of Ballantine et al. and Hanratty et al. or Tobben et al. Claims 2-4, 11, 18 and 20, which depend from Claim 1, are allowable over Cheng et al. in view of Ballantine et al. and Hanratty et al. or Tobben et al. for at least the same reasons as Claim 1.

Claims 12-17 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Ballantine et al. in view of Hanratty et al. or Tobben et al. and further in view of and Wolf.

Claims 12-17, which depend from Claim 1, are allowable over Cheng et al. and Ballantine et al. in view of Hanratty et al. or Tobben et al. for at least the same reasons as Claim 1. Because Wolf does not remedy the above-described deficiencies of Cheng et al. and Ballantine et al. in view

of Hanratty et al. or Tobben et al., Claims 12-17 are allowable over Cheng et al. and Ballantine et al. in view of Hanratty et al. or Tobben et al., and further in view of Wolf.

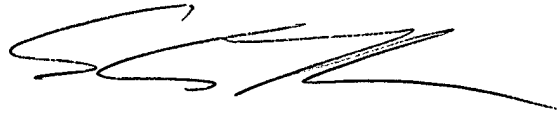
Claim 19 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Ballantine et al., in view of Hanratty et al. or Tobben et al., and further in view of Applicants Admitted Prior Art (AAPA).

Claim 19, which depends from Claim 1, is allowable over Cheng et al. and Ballantine et al. in view of Hanratty et al. or Tobben et al. for at least the same reasons as Claim 1. Because AAPA does not remedy the above-described deficiencies of Cheng et al. and Ballantine et al. in view of Hanratty et al. or Tobben et al., Claim 19 is allowable over Cheng et al. and Ballantine et al. in view of Hanratty et al. or Tobben et al., further in view of and AAPA.

CONCLUSION

Claims 1-4 and 11-20 are pending in the present application. Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned at (925) 895-3545.

Respectfully submitted,



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